

# ELECTRONIC CIRCUIT, ELECTRONIC DEVICE, AND ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

### 1. Field of Invention

[0001] The present invention relates to an electronic circuit, an electronic device, and an electronic apparatus.

### 2. Description of Related Art

[0002] In recent years, electro-optical devices using electro-optical elements such as organic EL (electroluminescent) elements have received attention. Since the organic EL elements are self-luminous elements, and thus do not require a backlight, it is possible to realize an electro-optical device having low power consumption, a wide angle of view and high contrast ratio.

[0003] Among such kinds of electro-optical devices, in an electro-optical device referred to as an "active matrix electro-optical device," pixel circuits for controlling driving current supplied to the organic EL elements are provided in a display panel unit thereof.

[0004] The pixel circuits include capacitors for storing a quantity of electric charge corresponding to data signals and transistors for controlling the driving current in accordance with the quantity of electric charge in the capacitors. See International Publication Pamphlet No. WO98/36406..

## SUMMARY OF THE INVENTION

[0005] However, in particular, in the pixel circuits including current-driven elements, such as organic EL elements as electro-optical elements, since unevenness in the characteristics of the transistors may directly affect the brightness of the electro-optical elements, it is necessary to suppress the unevenness in the characteristics of the transistors.

[0006] Therefore, the present invention provides an electronic circuit, an electronic device, and an electronic apparatus which are capable of suppressing the unevenness in the characteristics of transistors.

[0007] Further, for example, when current signals are used as data signals, in particular, time of writing data to the pixel circuits is lengthened, or power consumption is increased. Therefore, the present invention provides an electronic circuit, an electronic device, and an electronic apparatus which are suitable for shortening the data writing time or decreasing the power consumption when current signals are used as the data signals.

**[0008]** An electronic circuit according to the present invention includes: a first circuit unit through which a first current having a first current level passes; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current, having a second current level different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, at least one of the first circuit unit and the second circuit unit including unit elements connected in series or in parallel.

**[0009]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements in series or in parallel, it is possible to provide an electronic circuit capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0010]** An electronic circuit according to the present invention includes: a first circuit unit through which a first current having a first current level passes; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current, having a second current level different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, the first circuit unit including a plurality of unit elements connected in parallel.

**[0011]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in parallel, it is possible to provide an electronic circuit capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0012]** An electronic circuit according to the present invention includes: a first circuit unit through which a first current having a first current level passes; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current, having a second current level different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, the second circuit unit including a plurality of unit elements connected in series.

**[0013]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in series, it is possible to provide an electronic circuit capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0014]** An electronic circuit according to the present invention includes: a first circuit unit through which a first current having a first current level passes; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current, having a second current level different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, the first circuit unit including a plurality of unit elements connected in parallel and the second circuit unit includes a plurality of unit elements connected in series.

**[0015]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in parallel and connecting the unit elements of the second circuit unit in series, it is possible to provide an electronic circuit capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0016]** An electronic circuit according to the present invention includes: a first circuit unit through which a first current having a first current level passes; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element, wherein at least one of the first circuit unit and the second circuit unit includes a plurality of unit elements connected in series or in parallel and the electrical connections of the plurality of unit elements are controlled by a control element.

**[0017]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by using the number of unit elements constituting the first circuit unit and the second circuit unit in combination, it

is possible to provide an electronic circuit capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0018]** In the above electronic circuit, at least one of the plurality of unit elements is a unit element common to the first circuit unit and the second circuit unit.

**[0019]** According to this construction, a current mirror circuit can be constructed from the first circuit unit and the second circuit unit.

**[0020]** In the above electronic circuit, the plurality of unit elements have the same driving capability.

**[0021]** According to this construction, it is possible to enhance the mirror characteristic of the current mirror circuit.

**[0022]** In this electronic circuit, the plurality of unit elements are formed in a bundle.

**[0023]** According to this construction, the electronic circuit including the first circuit unit and the second circuit unit can be easily constructed.

**[0024]** In the above electronic circuit, the first current level is higher than the second current level.

**[0025]** According to this construction, the first current can be written to the capacitor element at a high speed.

**[0026]** In this electronic circuit, the second current level is higher than the first current level.

**[0027]** According to this construction, the current level of the first current can be amplified.

**[0028]** The above electronic circuit may include electronic elements supplied with the second current.

**[0029]** According to this construction, it is possible to provide an electronic circuit having the electronic elements that are driven on the basis of a current level different from the current level of the inputted current while suppressing an enlargement of the area occupied by constituent transistors.

**[0030]** In this electronic circuit, the electronic elements may be electro-optical elements or current-driven elements.

**[0031]** According to this construction, it is possible to provide an electronic circuit having the electro-optical elements or the current-driven elements that are driven on the basis

of a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

[0032] In the above electronic circuit, the electronic elements may be organic EL elements.

[0033] According to the above construction, it is possible to provide an electronic circuit having the organic EL elements that are driven on the basis of a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

[0034] An electronic device according to the present invention is provided with a first signal line, a second signal line, and a plurality of unit circuits, each of the plurality of unit circuits including: a switching element connected to the first signal line, wherein an on/off state of the switching element is controlled by switching signals supplied from the first signal line; a first circuit unit connected to the second signal line, a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current having a second current level, different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, at least one of the first circuit unit and the second circuit unit including unit elements connected in series or in parallel.

[0035] According to the above construction, since the writing of data signals to the capacitor element can be carried out by current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements in series or in parallel, it is possible to provide an electronic device capable of generating current having a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

[0036] An electronic device according to the present invention is provided with a first signal line, a second signal line, and a plurality of unit circuits, each of the plurality of unit circuits including: a switching element connected to the first signal line, an on/off state of the switching element being controlled by switching signals supplied from the first signal line; a first circuit unit connected to the second signal line, a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current

having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element, wherein the first circuit unit includes a plurality of unit elements connected in parallel.

**[0037]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in parallel, it is possible to provide an electronic device capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0038]** An electronic device according to the present invention is provided with a first signal line, a second signal line, and a plurality of unit circuits, each of the plurality of unit circuits including: a switching element connected to the first signal line, wherein an on/off state of the switching element is controlled by switching signals supplied from the first signal line; a first circuit unit connected to the second signal line, a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current having a second current level, different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, the second circuit unit including a plurality of unit elements connected in series.

**[0039]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in series, it is possible to provide an electronic device capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0040]** An electronic device according to the present invention is provided with a first signal line, a second signal line, and a plurality of unit circuits, each of the plurality of unit circuits including: a switching element connected to the first signal line, wherein an on/off state of the switching element is controlled by switching signals supplied from the first signal line; a first circuit unit connected to the second signal line, a first current having a first current level supplied from the second signal line passing through the first circuit unit by

switching on the switching element; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current, having a second current level different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, the first circuit unit comprising a plurality of unit elements connected in parallel and the second circuit unit including a plurality of unit elements connected in series.

**[0041]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by connecting the unit elements of the first circuit unit in parallel and connecting the unit elements of the second circuit unit in series, it is possible to provide an electronic device capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0042]** An electronic device according to the present invention is provided with a first signal line, a second signal line, and a plurality of unit circuits, each of the plurality of unit circuits including: a switching element connected to the first signal line, wherein an on/off state of the switching element is controlled by switching signals supplied from the first signal line; a first circuit unit connected to the second signal line, a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element; a capacitor element to store a quantity of electric charge corresponding to the first current level; and a second circuit unit to generate a second current having a second current level, different from the first current level, on the basis of the quantity of electric charge stored in the capacitor element, at least one of the first circuit unit and the second circuit unit including a plurality of unit elements connected in series or in parallel and the electrical connections of the plurality of unit elements being controlled by a control element.

**[0043]** According to the above construction, since the writing of data signals to the capacitor element can be carried out by means of the current signals, it is possible to suppress the unevenness in the characteristics of the unit elements. Furthermore, by using the number of unit elements constituting the first circuit unit and the second circuit unit in combination, it is possible to provide an electronic device capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0044]** In the above electronic device, at least one of the plurality of unit elements may be a unit element common to the first circuit unit and the second circuit unit.

**[0045]** According to the above construction, a current mirror circuit can be constructed from the first circuit unit and the second circuit unit.

**[0046]** In the above electronic device, the plurality of unit elements have the same driving capability.

**[0047]** According to the above construction, it is possible to enhance the mirror characteristic of the current mirror circuit.

**[0048]** In the above electronic device, the plurality of unit elements may be formed in a bundle.

**[0049]** According to this construction, the electronic device including the first circuit unit and the second circuit unit can be easily constructed.

**[0050]** In the above electronic device, the first current level is higher than the second current level.

**[0051]** According to the above construction, the first current can be written to the capacitor element at a high speed.

**[0052]** In the above electronic device, the second current level may be higher than the first current level.

**[0053]** According to the above construction, the current level of the first current can be amplified.

**[0054]** The above electronic device may include electronic elements supplied with the second current.

**[0055]** According to the above construction, it is possible to provide an electronic device having the electronic elements that are driven on the basis of a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0056]** In the above electronic device, the electronic elements may be electro-optical elements or current-driven elements.

**[0057]** According to the above construction, it is possible to provide an electronic device having the electro-optical elements or the current-driven elements that are driven on the basis of a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.



**[0058]** In the above electronic device, the electronic elements may be organic EL elements.

**[0059]** According to the above construction, it is possible to provide an electronic device having the organic EL elements that are driven on the basis of a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0060]** An electronic apparatus according to the present invention has mounted thereon the aforementioned electronic circuit.

**[0061]** According to the above construction, it is possible to provide an electronic apparatus in which the unevenness in the characteristics of transistors is suppressed. Furthermore, by connecting the unit elements in series or in parallel, it is possible to provide an electronic apparatus including the electronic circuit capable of generating current having a current level, different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

**[0062]** An electronic apparatus according to the present invention has mounted thereon the aforementioned electronic device.

**[0063]** According to the above construction, it is possible to provide an electronic apparatus in which the unevenness in the characteristics of transistors is suppressed. Furthermore, by connecting the unit elements in series or in parallel, it is possible to provide an electronic apparatus including the electronic device capable of generating current, having a current level different from the current level of the inputted current, while suppressing an enlargement of the area occupied by constituent transistors.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0064]** Fig. 1 is a circuitry block schematic illustrating a circuit configuration of an organic EL display device according to a first exemplary embodiment.

**[0065]** Fig. 2 is a circuitry block schematic illustrating an internal configuration of a display panel part and a data line driving circuit.

**[0066]** Fig. 3 is a circuit schematic of a pixel circuit for the purpose of explanation of the first exemplary embodiment.

**[0067]** Fig. 4 is a timing chart for explaining the operation of the pixel circuit according to the first exemplary embodiment.

**[0068]** Fig. 5 is a circuit schematic of a pixel circuit for the purpose of explanation of a second exemplary embodiment.

[0069] Fig. 6 is a timing chart for explaining the operation of the pixel circuit according to the second exemplary embodiment.

[0070] Fig. 7 is an equivalent circuit schematic of the pixel circuit for the purpose of explanation of the second exemplary embodiment.

[0071] Fig. 8 is an equivalent circuit schematic of the pixel circuit for the purpose of explanation of the second exemplary embodiment.

[0072] Fig. 9 is a perspective view illustrating a configuration of a mobile personal computer for the purpose of explanation of a third exemplary embodiment.

[0073] Fig. 10 is a perspective view illustrating a configuration of a mobile phone for the purpose of explanation of the third exemplary embodiment.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

##### [0074] First Exemplary Embodiment

[0075] Now, a first exemplary embodiment of the present invention will be described with reference to Figs. 1 to 4. Fig. 1 is a circuitry block schematic illustrating a circuit configuration of an organic EL display device as an electronic device. Fig. 2 is a circuitry block schematic illustrating an internal configuration of a display panel unit and a data line driving circuit. Fig. 3 is a circuit schematic of a pixel circuit. Fig. 4 is a timing chart illustrating the operation of the pixel circuit.

[0076] An organic EL display device 10 includes, as shown in Fig. 1, a control circuit 11, a display panel unit 12, a scanning line driving circuit 13, and a data line driving circuit 14.

[0077] The control circuit 11, the scanning line driving circuit 13, and the data line driving circuit 14 of the organic EL display device 10 may be constructed using an independent electronic component, respectively.

[0078] For example, the control circuit 11, the scanning line driving circuit 13, and the data line driving circuit 14 may be constructed using one chip semiconductor integrated circuit device, respectively.

[0079] Otherwise, all or some of the control circuit 11, the scanning line driving circuit 13, and the data line driving circuit 14 may be constructed using a programmable IC chip, and the functions thereof may be executed as software by programs written in the IC chip.

[0080] The control circuit 11 generates scanning control signals and data control signals for displaying desired images in the display panel unit 12 on the basis of image data

outputted from an external device (not shown). Further, the control circuit 11 outputs the scanning control signals to the scanning line driving circuit 13, and outputs the data control signals to the data line driving circuit 14.

**[0081]** As shown in Fig. 2, pixel circuits 20 as a plurality of electronic circuits or a plurality of unit circuits having organic EL elements 21 as electronic elements or current-driven elements whose light emitting layers are made of organic materials are arranged in a matrix in the display panel unit 12. That is, the pixel circuits 20 are arranged at positions corresponding to the intersected portions of M data lines  $X_m$  ( $m = 1$  to M; m is an integer) extending in a column direction and N scanning lines  $Y_n$  ( $n = 1$  to N; n is an integer) extending in a row direction. Further, in this exemplary embodiment, the organic EL elements 21 are organic EL elements, which properly emit light by a driving current  $I_{el}$  as a second current, having an intensity of about 1/25th of the intensity of data current  $I_{data}$  as first current, generated in the data line driving circuit 14. Furthermore, transistors, which will be described later disposed in the respective pixel circuits 20 comprise TFTs (Thin Film Transistor), respectively.

**[0082]** The scanning line driving circuit 13 selects one scanning line of the N scanning lines  $Y_n$  provided in the display panel unit 12 on the basis of the scanning control signals outputted from the control circuit 11, and then outputs scanning signals to the selected scanning line.

**[0083]** The data line driving circuit 14 includes a plurality of single line drivers 23. Each of the single line drivers 23 is connected to the data line  $X_m$  provided in the display panel unit 12. Each of the single line drivers 23 generates data currents  $I_{data1}$  to  $I_{datam}$ , respectively, on the basis of the data control signals outputted from the control circuit 11. Further, the single line drivers 23 supply the generated data currents  $I_{data1}$  to  $I_{datam}$ , to the corresponding pixel circuits 20, through the corresponding data lines  $X_1$  to  $X_m$ , respectively. By setting up the internal states of the corresponding pixel circuits 20 in accordance with the data currents  $I_{data1}$  to  $I_{datam}$ , respectively, the pixel circuits 20 control the driving currents  $I_{el}$  flowing in the organic EL elements 21 to control gray scales in the brightness of the corresponding organic EL elements 21, respectively.

**[0084]** The pixel circuits 20 of the organic EL display device 10 constructed like the above will be described below with reference to Fig. 3. On the other hand, since the circuit configurations of the respective pixel circuits 20 are the same, only the pixel circuit 20

arranged at the intersected portion of the m-th data line  $X_m$  and the n-th scanning line  $Y_n$  will be described, for the purpose of convenience of explanation.

**[0085]** The pixel circuit 20 include five driving transistors  $Q_s$ , five current supply transistors  $Q_p$ , first and second switching transistors  $Q_1$ ,  $Q_2$ , and a storage capacitor  $C_n$ . Further, the driving transistors  $Q_s$  and the current supply transistors  $Q_p$ , the first switching transistor  $Q_1$  and the storage capacitor  $C_n$  correspond to the unit elements, the switching element, and the capacitor element described in the claims, respectively. Further, conductive types of the driving transistors  $Q_s$  and the current supply transistors  $Q_p$  are p type (p channel), respectively. Furthermore, conductive types of the first and second switching transistors  $Q_1$ ,  $Q_2$  are n type (n channel), respectively.

**[0086]** The respective driving transistors  $Q_s$  are transistors functioning as driving transistors whose gain factor as driving capability is set to be  $\beta_s$ . The respective current supply transistors  $Q_p$  are transistors functioning as switching elements whose gain factor as driving capability is set to be  $\beta_p$ . Further, in this exemplary embodiment, the gain factor  $\beta_s$  of the driving transistors  $Q_s$  is set to be equal to the gain factor  $\beta_p$  of the current supply transistors  $Q_p$ .

**[0087]** The first and second switching transistors  $Q_1$ ,  $Q_2$  are transistors functioning as switching elements whose on/off state is controlled in accordance with the scanning signals supplied from the scanning line driving circuit 13.

**[0088]** The five driving transistors  $Q_s$  are mutually connected in series. That is, drains of the respective driving transistor  $Q_s$  are connected to sources of the driving transistor  $Q_s$  arranged adjacent to the respective driving transistors  $Q_s$ . Further, among the five driving transistors  $Q_s$ , a driving transistor  $Q_s$  whose source is not connected to the drain of the adjacent driving transistor  $Q_s$  is connected to a power source line VL for supplying driving voltage Vdd. Furthermore, among the five driving transistors  $Q_s$ , a driving transistor  $Q_s$  whose drain is not connected to the source of the adjacent driving transistor  $Q_s$  is connected to an anode of the organic EL element 21. A cathode of the organic EL element 21 is grounded.

**[0089]** Furthermore, the respective gates of the five driving transistors  $Q_s$  connected in series are connected to the respective gates of the current supply transistors  $Q_p$  in common. The five driving transistors  $Q_s$  connected in series like the above constitute the driving current generation circuit unit 30 as a second circuit unit.

[0090] Furthermore, the storage capacitor  $C_n$  is connected between the mutually connected gates of the five driving transistors  $Q_s$  constituting the driving current generation circuit unit 30 and the power source line VL.

[0091] The five current supply transistors  $Q_p$  are mutually connected in parallel. That is, the respective sources, the respective gates, and the respective drains of the five current supply transistors  $Q_p$  are mutually connected, respectively. Further, the respective drains of the current supply transistors  $Q_p$  are mutually connected and they are connected to the power source line VL. The respective gates of the current supply transistors  $Q_p$  are mutually connected and they are connected to the respective gates of the five driving transistors  $Q_s$  constituting the driving current generation circuit unit 30.

[0092] Furthermore, the respective drains of the current supply transistors  $Q_p$  are mutually connected and they are connected to the first switching transistor  $Q_1$ . The source of the first switching transistor  $Q_1$  is connected to the data line  $X_m$ , which is electrically connected to the data line driving circuit 14. The gate of the first switching transistor  $Q_1$  is connected to a first sub-scanning line  $Y_{n1}$  as a first signal line, which is connected to the scanning line driving circuit 13. As described above, the five current supply transistors  $Q_p$ , mutually connected in parallel, constitute the current supply circuit unit 40 as a first circuit unit. The driving current generation circuit unit 30 and the current supply circuit unit 40 constitute a current value converting device.

[0093] Furthermore, the second switching transistor  $Q_2$  is connected between the respective drains of the five current supply transistors  $Q_p$  constituting the current supply circuit unit 40 and the respective gates of the current supply transistors  $Q_p$ . The gate of the second switching transistor  $Q_2$  is connected to a second sub-scanning line  $Y_{n2}$  as a second signal line, which is electrically connected to the scanning line driving circuit 13. That is, by switching on the second switching transistor  $Q_2$ , the five current supply transistors  $Q_p$  constituting the current supply circuit unit 40 are connected to diodes, respectively. Then, by allowing the respective current supply transistors  $Q_p$  to be connected to diodes, the respective current supply transistors  $Q_p$  and the five driving transistors  $Q_s$  constituting the driving current generation circuit unit 30 constitute a current mirror circuit through the storage capacitor  $C_n$ . Furthermore, the first and second sub-scanning lines  $Y_{n1}$ ,  $Y_{n2}$  constitute the scanning line  $Y_n$ .

[0094] Now, the operation of the driving current generation circuit unit 30 and the current supply circuit unit 40 constructed like the above will be described.

[0095] In general, when a plurality of transistors, having the same gain factor are mutually connected in series, it is known that the resultant gain factor of the transistors connected in series is a value obtained by dividing the gain factor of the respective transistors by the number of connected transistors. That is, supposing that the number of transistors connected in series is  $n$  and the gain factor of the respective transistors is  $\beta_s$ , the resultant gain factor  $\beta_{so}$  of the transistors mutually connected in series is expressed as follows.

$$[0096] \quad \beta_{so} = \beta_s/n$$

[0097] Therefore, the resultant gain factor  $\beta_{so}$  of the driving current generation circuit unit 30 including the five driving transistors  $Q_s$  having a gain factor of  $\beta_s$  in this exemplary embodiment is expressed as follows.

$$[0098] \quad \beta_{so} = \beta_s/5$$

[0099] Furthermore, when a plurality of transistors, having the same gain factor are mutually connected in parallel, it is known that the resultant gain factor of the transistors mutually connected in parallel is a value obtained by multiplying the gain factor of the respective transistors by the number of connected transistors. That is, supposing that the number of transistors connected in parallel is  $n$  and the gain factor of the respective transistors is  $\beta_p$ , the resultant gain factor  $\beta_{po}$  of the transistors connected in parallel is expressed as follows.

$$[0100] \quad \beta_{po} = \beta_p \cdot n$$

[0101] Therefore, the resultant gain factor  $\beta_{po}$  of the current supply circuit unit 40 including the five current supply transistors  $Q_p$  having a gain factor of  $\beta_p$  in this exemplary embodiment is expressed as follows.

$$[0102] \quad \beta_{po} = \beta_p \cdot 5$$

[0103] Here, supposing that the respective resultant gain factors of the driving current generation circuit unit 30 and the current supply circuit unit 40 are denoted as  $\beta_{so}$  and  $\beta_{po}$ , the relative ratio of the data current  $I_{data}$  and the driving current  $I_{el}$  is expressed as the following equation.

$$[0104] \quad I_{data} : I_{el} = \beta_{po} : \beta_{so}$$

[0105] Here, since the resultant gain factor  $\beta_{so}$  of the driving current generation circuit unit 30 is  $\beta_s/5$  and the resultant gain factor  $\beta_{po}$  of the current supply circuit unit 40 is  $5\beta_p$ , the relative ratio of the data current  $I_{data}$  and the driving current  $I_{el}$  is expressed as follows.

$$[0106] \quad I_{data} : I_{el} = 5\beta_p : \beta_s/5$$

[0107] Since the gain factor  $\beta_p$  of the current supply transistors  $Q_p$  is set to be equal to the gain factor  $\beta_s$  of the driving transistors  $Q_s$  as described above, the above equation is expressed as follows.

$$[0108] \quad I_{data} : I_{el} = \beta_{po} : \beta_{so}$$

$$[0109] \quad = 5 : 1/5$$

[0110] Therefore, the data current  $I_{data}$  is expressed as the following equation.

$$I_{data} = 25I_{el}$$

[0111] Therefore, since the pixel circuits 20 of the present invention can be supplied with the data current  $I_{data}$ , having a current level twenty five times greater than the current level of the driving current  $I_{el}$ , the first current level for the data current  $I_{data}$  can be written into the storage capacitor  $C_n$  at a correspondingly higher speed. Furthermore, since the writing of data onto storage capacitor  $C_n$  is carried out using the data current  $I_{data}$  that is a current signal, it is possible to suppress the unevenness in the characteristics such as a threshold voltage of the driving transistors  $Q_s$  for every pixel circuit 20.

[0112] Furthermore, since the driving transistors  $Q_s$  and the current supply transistors  $Q_p$  are formed to have the same gain factor, it is possible to enhance the accuracy in the mirror characteristic, compared with a case where the current mirror circuit is constructed using different gain factors.

[0113] Next, an occupied area of the overall transistors arranged in the pixel circuit 20 including the driving current generation circuit unit 30 and the current supply circuit unit 40 is calculated.

[0114] First, the occupied area  $S_1$  of the five driving transistors  $Q_s$  constituting the driving current generation circuit unit 30 is calculated. In general, when the channel lengths of transistors are the same, it is known that the occupied area of the transistors is proportional to the gain factor. Since the gain factors  $\beta_s$  of the respective driving transistors  $Q_s$  are the same, if the respective occupied areas of the respective driving transistors  $Q_s$  are denoted as  $S_{Qs}$ , the occupied area  $S_1$  of the driving current generation circuit unit 30 is expressed as follows.

$$[0115] \quad S_1 = 5S_{Qs}$$

[0116] Next, the occupied area  $S_2$  of the five current supply transistors  $Q_p$  constituting the current supply circuit unit 40 is calculated. Since the gain factors  $\beta_p$  of the respective current supply transistors  $Q_p$  are the same, if the respective occupied areas of the

respective current supply transistors  $Q_p$  are  $S_{Qp}$ , the occupied area  $S_2$  of the five current supply transistors  $Q_p$  is expressed as follows.

$$[0117] \quad S_2 = 5S_{Qp}$$

[0118] Therefore, if the occupied areas of the first and second switching transistors  $Q_1$ ,  $Q_2$  are  $S_{Q1}$  and  $S_{Q2}$ , respectively, the occupied area  $S_t$  of the overall transistors provided in the pixel circuit 20 is expressed as follows.

$$[0119] \quad S_t = 5S_{Qs} + 5S_{Qp} + S_{Q1} + S_{Q2}$$

[0120] Here, as described above, since the gain factor  $\beta_s$  of the driving transistors  $Q_s$  and the gain factor  $\beta_p$  of the current supply transistors  $Q_p$  are set to be equal to each other, the occupied area  $S_{Qs}$  of the driving transistors  $Q_s$  and the occupied area  $S_{Qp}$  of the current supply transistors  $Q_p$  are equal to each other. Further, the first and second switching transistors  $Q_1$ ,  $Q_2$  are transistors functioning as switching elements, as described above. Therefore, it is supposed that the occupied area  $S_{Q1}$  of the first switching transistor  $Q_1$  and the occupied area  $S_{Q2}$  of the second switching transistor  $Q_2$  are equal to each other, and supposed that the occupied areas  $S_{Q1}$ ,  $S_{Q2}$  are equal to the occupied areas  $S_Q$  of the driving transistors  $Q_s$  and the current supply transistors  $Q_p$ . By doing so, if the occupied area of the driving transistors  $Q_s$  is  $S_{Qs}$ , the occupied area  $S_t$  of the overall transistors in the pixel circuit 20 is expressed as follows.

$$[0121] \quad S_t = 5S_{Qs} + 5S_{Qp} + S_{Q1} + S_{Q2}$$

$$[0122] \quad = 12S_{Qs}$$

[0123] Next, an occupied area  $A_o$  of the overall transistors in a pixel circuit in which the driving current generation circuit unit 30 includes one driving transistor  $Q_s$ , the current supply circuit unit 40 includes one current supply transistor  $Q_p$ , and other first and second switching transistors  $Q_1$ ,  $Q_2$  are arranged similarly to the pixel circuit 20 is calculated. In this regard, it is supposed that the gain factor of the current supply transistor  $Q_p$  is twenty five times greater than the gain factor of the driving transistor  $Q_s$ . By doing so, the data current  $I_{data}$ , having the same current level as the pixel circuit 20, can be supplied to the storage capacitor  $C_n$ .

[0124] By doing so, as described above, since the occupied area of transistors is directly proportional to the gain factor, the relationship between the occupied area  $S_{Qp}$  of the current supply transistor  $Q_p$  and the occupied area  $S_{Qs}$  of the driving transistor  $Q_s$  is expressed as follows.

$$[0125] \quad S_{Qp} = 25S_{Qs}$$



[0126] Therefore, the occupied area  $A_o$  is expressed as follows.

$$[0127] \quad A_o = SQ_p + SQ_s + SQ_1 + SQ_2$$

$$[0128] \quad = 25SQ_s + SQ_s + SQ_1 + SQ_2$$

$$[0129] \quad = 26SQ_s + SQ_1 + SQ_2$$

[0130] Here, similarly to the occupied area  $St$  of the overall transistors provided in the pixel circuit 20, it is supposed that the respective occupied areas  $SQ_1$  and  $SQ_2$  of the first and second switching transistors  $Q_1$ ,  $Q_2$  are equal to each other. Then, supposing that the respective areas  $SQ_1$  and  $SQ_2$  of the first and second switching transistors  $Q_1$ ,  $Q_2$  are equal to the occupied area  $SQ_s$  of the driving transistor  $Q_s$ , the occupied area  $A_o$  is expressed as follows.

$$[0131] \quad A_o = 26SQ_s + SQ_1 + SQ_2$$

$$[0132] \quad = 28SQ_s$$

[0133] From the above result, compared with the pixel circuit in which the driving current generation circuit unit 30 includes one driving transistor  $Q_s$  and the current supply circuit unit 40 includes one current supply transistor  $Q_p$ , the pixel circuit 20 shown in Fig. 3 can be supplied with the same quantity of the data current  $I_{data}$  as the driving current  $I_{el}$  and the occupied area of transistors thereof can be reduced by about 60%. The reduction rate of the occupied area,  $So$  of the transistors, is increased with increase in the relative ratio of the data current  $I_{data}$  and the driving current  $I_{el}$ . For this reason, the pixel circuit in which the driving current generation circuit unit 30 includes a plurality of driving transistors  $Q_s$  and the current supply circuit unit 40 includes a plurality of current supply transistors  $Q_p$  can have larger aperture ratio.

[0134] Next, a method of driving the pixel circuit 20 including the driving current generation circuit unit 30 and the current supply circuit unit 40 will be described with reference to Fig. 4. Fig. 4 is a timing chart of a first scanning signal  $SC_1$  and a second scanning signal  $SC_2$  as switching signals supplied to the first and second switching transistors  $Q_1$ ,  $Q_2$  and the driving current  $I_{el}$  flowing in the organic EL elements 21.

[0135] Further, in Fig. 4,  $T_c$ ,  $T_1$  and  $T_2$  denote a driving cycle, a data-writing period, and a light-emitting period, respectively. The driving cycle  $T_c$  includes the data-writing period  $T_1$  and the light-emitting period  $T_2$ . The driving cycle  $T_c$  means a cycle in which the gray scales in the brightness of the organic EL elements 21 is updated by one turn and is the same as a so-called frame cycle.

**[0136]** First, for a predetermined data-writing period  $T1$ , the first and second scanning signals  $SC1$ ,  $SC2$  for switching on the first and second switching transistors  $Q1$ ,  $Q2$  are supplied through the first and second sub-scanning lines  $Yn1$ ,  $Yn2$  from the scanning line driving circuit 13, respectively. When the first and second scanning signals  $SC1$ ,  $SC2$  for switching on the first and second switching transistors  $Q1$ ,  $Q2$  are supplied, the first and second switching transistors  $Q1$ ,  $Q2$  are switched on for the data-writing period  $T1$ , respectively. Accordingly, the data current  $I_{datam}$  is supplied to the pixel circuit 20 and the five current supply transistors  $Qp$ , constituting the current supply circuit unit 40, are connected to diodes. Then, the current supply transistors  $Qp$  and the five driving transistors  $Qs$ , constituting the driving current generation circuit unit 30, are electrically connected one another to construct the current mirror circuit. By doing so, the data current  $I_{datam}$  passes through the current supply circuit unit 40, and a quantity of electric charge corresponding to the current level of the data current  $I_{datam}$  as the first current level is stored in the storage capacitor  $Cn$ . As a result, the voltage corresponding to the quantity of electric charge stored in the storage capacitor  $Cn$  is applied between the respective gates/sources of the five driving transistors  $Qs$  constituting the driving current generation circuit unit 30.

**[0137]** Next, for a predetermined light-emitting period  $T2$  after the data-writing period  $T1$ , the first and second scanning signals  $SC1$ ,  $SC2$  for switching off the first and second switching transistors  $Q1$ ,  $Q2$  are supplied through the first and second sub-scanning lines  $Yn1$ ,  $Yn2$  from the scanning line driving circuit 13, respectively. When the first and second scanning signals  $SC1$ ,  $SC2$  for switching off the first and second switching transistors  $Q1$ ,  $Q2$  are supplied, the first and second switching transistors  $Q1$ ,  $Q2$  are switched off for the light-emitting period  $T2$ . Accordingly, the voltage corresponding to the quantity of electric charge stored in the storage capacitor  $Cn$  is applied between the respective gates/sources of the five driving transistors  $Qs$  constituting the driving current generation circuit unit 30. Then, the respective driving transistors  $Qs$  generate the driving current  $I_{el}$  having intensity based on the voltage corresponding to the quantity of electric charge stored in the storage capacitor  $Cn$ . At that time, the current level of the driving current  $I_{el}$  generated in the driving current generation circuit unit 30 is changed into  $1/25$ th of the data current  $I_{data}$ .

**[0138]** Further, although it is preferable that the first and second switching transistors  $Q1$ ,  $Q2$  be switched on for the data-writing period  $T1$  and switched off for the light-emitting period  $T2$ , they are not limited thereto.

**[0139]** (1) In this exemplary embodiment like the above, the driving current generation circuit unit 30 is constructed by connecting in series the five driving transistors  $Q_s$  having the same gain factor  $\beta_s$ . Further, the current supply circuit unit 40 is constructed by connecting in parallel the five current supply transistors  $Q_p$  having the same gain factor  $\beta_p$ . Also, by connecting the respective gates of the driving transistors  $Q_s$  constituting the driving current generation circuit unit 30 and the respective gates of the current supply transistors  $Q_p$  constituting the current supply circuit unit 40, the driving transistors  $Q_s$  and the current supply transistors  $Q_p$  constitute the current mirror circuit. Furthermore, the respective gates of the driving transistors  $Q_s$  are connected to the storage capacitor  $C_n$  for storing a quantity of electric charge corresponding to the data current  $I_{data}$ . Furthermore, the current supply circuit unit 40 is electrically connected to the data line  $X_m$  for supplying the data current  $I_{data}$ . Furthermore, the driving current  $I_{el}$  generated in the driving current generation circuit unit 30 is supplied to the organic EL elements 21.

**[0140]** Accordingly, the current level of the data current  $I_{data}$  can be set to be twenty five times greater than the driving current  $I_{el}$ . Therefore, the data current  $I_{data}$  can be written to the storage capacitor  $C_n$  at a correspondingly higher speed. Furthermore, since the writing of data to the storage capacitor  $C_n$  is carried out using the data current  $I_{data}$  which is a current signal, it is possible to suppress the unevenness in characteristics such as a threshold voltage of the driving transistors  $Q_s$  for every pixel circuit 20.

**[0141]** (2) Further, in this exemplary embodiment, the current mirror circuit is constructed using the method of connecting in parallel and in series the transistors having a predetermined gain factor, that is, using a method of combining unit elements. By doing so, compared with a case where transistors having different gain factors constitute the current mirror circuit, it is possible to improve the accuracy in the mirror characteristics.

**[0142]** (3) Further, in this exemplary embodiment, the driving current generation circuit unit 30 is constructed by connecting in series the five driving transistors  $Q_s$  having the same gain factor  $\beta_s$ . Furthermore, the current supply circuit unit 40 is constructed by connecting in parallel the five current supply transistors  $Q_p$  having the same gain factor  $\beta_p$ . Accordingly, it is possible to provide a pixel circuit capable of suppressing deterioration of the aperture ratio, while supplying the data current  $I_{data}$  having the current level twenty five times greater than the driving current  $I_{el}$ .

**[0143]** Second Exemplary Embodiment

[0144] Next, a second exemplary embodiment according to the present invention will be described with reference to Figs. 5 to 8. Further, in this exemplary embodiment, like reference numerals denote elements similar to those of the first exemplary embodiment, and the detailed description thereof will be omitted.

[0145] Fig. 5 is a circuit schematic of a pixel circuit 50 provided in the display panel unit 12 of the organic EL display device 10. Fig. 6 is a timing chart illustrating the operation of the pixel circuit. Figs. 7 and 8 are equivalent circuit schematics of the pixel circuit 50, respectively.

[0146] The pixel circuit 50 includes a current control circuit unit 60 combining the operation of the driving current generation circuit unit 30 with the current supply circuit unit 40 described in the first exemplary embodiment. Specifically, the pixel circuit 50 includes five transistors Qd1 to Qd5 functioning as driving transistors, first to seventh switching transistors Q1 to Q7 functioning as switching elements, a storage capacitor Cn, and an organic EL element 21. Further, the fourth to seventh switching transistors Q4 to Q7 of the first to seventh switching transistors Q1 to Q7 correspond to the control element recited in the Claims.

[0147] Conductive types of the first to fifth transistors Qd1 to Qd5 are all p type (p channel). Further, conductive types of the first to seventh switching transistors Q1 to Q7 are all n type (n channel). The first to fifth transistors Qd1 to Qd5 are set to have the same gain factor  $\beta_d$ . The on/off state of the first to seventh switching transistors Q1 to Q7 are controlled in accordance with the scanning signals supplied from the scanning line driving circuit 13, respectively.

[0148] The source of the first transistor Qd1, among the first to fifth transistors Qd1 to Qd5, is connected to the power source line VL for supplying the driving voltage Vdd. The drain of the first transistor Qd1 is connected to one electrode of the source and the drain of the second transistor Qd2. The source of the first transistor Qd1 is connected through the fourth switching transistor Q4 to the electrode of the second transistor Qd2, which are not connected to the drain of the first transistor Qd1.

[0149] The source or the drain of the second transistor Qd2, which is connected to the fourth switching transistor Q4, is connected to the drain or the source of the third transistor Qd3. The electrode of the second transistor Qd2, which is not connected to the drain or the source of the third transistor Qd3, is connected to the source or the drain of the sixth switching transistor Q6. The electrode of the sixth switching transistor Q6, which is not

connected to the source or the drain of the second transistor Qd2, is connected to the electrode of the third transistor Qd3, which is not connected to the second transistor Qd2.

**[0150]** The electrode of the third transistor Qd3, which is connected to the source or the drain of the sixth switching transistor Q6, is connected to the drain or the source of the fourth transistor Qd4. The electrode of the third transistor Qd3, which is not connected to the drain or the source of the fourth transistor Qd4, is connected to the source or the drain of the fifth switching transistor Q5. The electrode of the fifth switching transistor Q5, which is not connected to the source or the drain of the third transistor Qd3, is connected to the electrode of the fourth transistor Qd4, which is not connected to the third transistor Qd3.

**[0151]** The source or the drain of the fourth transistor Qd4, which is connected to the source or the drain of the fifth switching transistor Q5, is connected to the source of the fifth transistor Qd5. The electrode of the fourth transistor Qd4, which is not connected to the drain or the source of the fifth switching transistor Q5, is connected to the source or the drain of the seventh switching transistor Q7. The electrode of the seventh switching transistor Q7, which is not connected to the fourth transistor Qd4, is connected to the drain of the fifth transistor Qd5. The drain of the fifth transistor Qd5 is connected to the drain of the first switching transistor Q1. The source of the first switching transistor Q1 is connected to the data line Xm, which is electrically connected to the data line driving circuit 14.

**[0152]** Furthermore, the respective gates of the fourth to seventh switching transistors Q4 to Q7 are mutually connected and they are connected to a third sub-scanning line Yn3 in common.

**[0153]** Also, the first to fifth transistors Qd1 to Qd5 and the fourth to seventh switching transistors Q4 to Q7 constitute the current control circuit unit 60.

**[0154]** Furthermore, the respective gates of the first to fifth transistors Qd1 to Qd5 constituting the current control circuit unit 60 are mutually connected in common and they are connected to the storage capacitor Cn and the drain of the second switching transistor Q2. The electrode of the storage capacitor Cn, which is not connected to the respective gates of the first to fifth transistors Qd1 to Qd5, is connected to the power source line VL. Furthermore, the source of the second switching transistor Q2 is connected to the drain of the first switching transistor Q1 and the drain of the third switching transistor Q3, respectively. The gate of the second switching transistor Q2 and the gate of the first switching transistor Q1 are mutually connected in common, and they are connected to the first sub-scanning line Yn1. The gate of the third switching transistor Q3 is connected to the second sub-scanning

line Yn2. The source of the third switching transistor Q3 is connected to the anode of the organic EL element 21. The cathode of the organic EL element 21 is grounded.

[0155] Next, the operation of the pixel circuit 50 including the current control circuit unit 60 will be described.

[0156] The current control circuit unit 60 constituting the pixel circuit 50 is set to vary the resultant gain factor  $\beta_o$  by controlling the respective on/off state of the fourth to seventh switching transistors Q4 to Q7 in accordance with a third scanning signal SC3 supplied from the scanning line driving circuit 13. Specifically, when the current control circuit unit 60 supplies the data current  $I_{data}$  to the pixel circuit 50, the third scanning signal SC3, for switching on the fourth to seventh switching transistors Q4 to Q7, is supplied to the respective gates of the fourth to seventh switching transistors Q4 to Q7 from the scanning line driving circuit 13. By doing so, the fourth to seventh transistors Q4 to Q7 are switched on, respectively.

[0157] At that time, the first to fifth transistors Qd1 to Qd5, constituting the current control circuit unit 60, are mutually connected in parallel. The resultant gain factor  $\beta_{po}$  of the current control circuit unit 60 in which the first to fifth transistors Qd1 to Qd5 are mutually connected in parallel is expressed as follows, using the gain factor  $\beta_d$  of the first to fifth transistors Q1 to Q5.

$$[0158] \quad \beta_{po} = 5\beta_d$$

[0159] Furthermore, when the current control circuit unit 60 generates the driving current  $I_{el}$ , the third scanning signal SC3 for switching off the fourth to seventh switching transistors Q4 to Q7 is supplied to the respective gates of the fourth to seventh switching transistors Q4 to Q7 from the scanning line driving circuit 13. By doing so, the fourth to seventh transistors Q4 to Q7 are switched off, respectively.

[0160] At that time, the first to fifth transistors Qd1 to Qd5 constituting the current control circuit unit 60 are mutually connected in series. The resultant gain factor  $\beta_{po}$  of the current control circuit unit 60 in which the first to fifth transistors Qd1 to Qd5 are mutually connected in series is expressed as follows, using the gain factor  $\beta_d$  of the first to fifth transistors Q1 to Q5.

$$[0161] \quad \beta_{po} = \beta_d/5$$

[0162] Therefore, using the resultant gain factor  $\beta_{po}$  when the first to fifth transistors Qd1 to Qd5 are mutually connected in parallel and the resultant gain factor  $\beta_{so}$

when the first to fifth transistors Qd1 to Qd5 are mutually connected in series, the ratio of the data current  $I_{data}$  to the driving current  $I_{el}$  is expressed as the following equation.

$$[0163] \quad I_{data} : I_{el} = \beta_{po} : \beta_{so}$$

$$[0164] \quad = 5\beta_d : \beta_d/5$$

$$[0165] \quad = 5 : 1/5$$

[0166] Therefore, the data current  $I_{data}$  is expressed as the following equation.

$$[0167] \quad I_{data} = 25I_{el}$$

[0168] Therefore, the pixel circuit 50 of this exemplary embodiment can be supplied with the data current  $I_{data}$  having a current level twenty five times greater than the current level of the driving current  $I_{el}$ . That is, since the current level of the data current  $I_{data}$  is twenty five times higher than the current level of the driving current  $I_{el}$ , the data current  $I_{data}$  can be written into the storage capacitor  $C_n$  at a correspondingly higher speed. Furthermore, since the writing of data to storage capacitor  $C_n$  is carried out using the data current  $I_{data}$  which is a current signal, it is possible to suppress the unevenness in characteristics such as threshold voltages of the first to fifth transistors Qd1 to Qd5 for every pixel circuits 50.

[0169] Next, the occupied area of the overall transistors provided in the pixel circuit 50 including the current control circuit unit 60 is calculated.

[0170] If the respective occupied areas of the first to fifth transistors Qd1 to Qd5 are denoted as  $S_{Qd1}$  to  $S_{Qd5}$  and the respective occupied areas of the first to seventh switching transistors Q1 to Q7 are denoted as  $S_{Q1}$  to  $S_{Q7}$ , the occupied area  $S_t$  of the overall transistors in the pixel circuit 50 is expressed as follows.

$$[0171] \quad S_t = S_{Qd1} + S_{Qd2} + S_{Qd3} + S_{Qd4} + S_{Qd5} + S_{Q1} + S_{Q2} + S_{Q3} + S_{Q4} + S_{Q5} + S_{Q6} + S_{Q7}$$

[0172] Here, since the gain factors  $\beta_d$  of the first to fifth transistors Qd1 to Qd5 are the same value, the occupied areas  $S_{Qd1}$  to  $S_{Qd5}$  of the first to fifth transistors Qd1 to Qd5 are the same value. Further, since the first to seventh switching transistors Q1 to Q7 are transistors functioning as switching elements, it is supposed that the occupied areas thereof are the same value.

[0173] Therefore, if the occupied area of the first to fifth transistors Qd1 to Qd5 is denoted as  $S_{Qd}$  and the occupied area of the first to seventh switching transistors Q1 to Q7 is denoted as  $S_{Qo}$ , respectively, the occupied area  $S_t$  of the overall transistors provided in the pixel circuit 50 is as follows.

$$[0174] \quad St = SQd1 + SQd2 + SQd3 + SQd4 + SQd5 + SQ1 + SQ2 + SQ3 + SQ4 + SQ5 + SQ6 + SQ7$$

$$[0175] \quad = 5SQd + 7SQo$$

[0176] Here, it is supposed that the occupied area  $SQt$  of the first to seventh switching transistors  $Q1$  to  $Q7$  is equal to the occupied area  $SQd$  of the first to fifth transistors  $Qd1$  to  $Qd5$ . Then, if the occupied areas of the first to fifth transistors  $Qd1$  to  $Qd5$  are denoted as  $SQo$ , the occupied area  $St$  of the overall transistors provided in the pixel circuit 50 is expressed as follows.

$$[0177] \quad St = 5SQd + 7SQo$$

$$[0178] \quad = 12SQd$$

[0179] Therefore, advantages similar to those of the first exemplary embodiment can be obtained from the pixel circuit 50 including the current control circuit unit 60.

[0180] Next, a method of driving the pixel circuit 50 including the current control circuit unit 60 will be described with reference to Figs. 6 to 8. Fig. 6 is a timing chart of the first, second and third scanning signals  $SC1$ ,  $SC2$ ,  $SC3$  supplied to the first, second and third switching transistors  $Q1$ ,  $Q2$ ,  $Q3$ , and the driving current  $Iel$  flowing in the organic EL element 21.

[0181] First, for the predetermined data-writing period  $T1$ , the first scanning signal  $SC1$  for switching on the first and second switching transistors  $Q1$ ,  $Q2$  is supplied through the first sub-scanning line  $Yn1$  from the scanning line driving circuit 13. Further, at that time, the second scanning signal  $SC2$  for switching off the third switching transistor  $Q3$  is supplied through the second sub-scanning line  $Yn2$  from the scanning line driving circuit 13. Furthermore, the third scanning signal  $SC3$  for switching on the fourth to seventh switching transistors  $Q4$  to  $Q7$  is supplied through the third sub-scanning line  $Yn3$  from the scanning line driving circuit 13.

[0182] When the first scanning signal  $SC1$  for switching on the first and second switching transistors  $Q1$ ,  $Q2$  is supplied, the first and second switching transistors  $Q1$ ,  $Q2$  are switched on, respectively. Further, when the second scanning signal  $SC2$  for switching off the third switching transistor  $Q3$  is supplied, the third switching transistor  $Q3$  is switched off. Furthermore, when the third scanning signal  $SC3$  for switching on the fourth to seventh switching transistors  $Q4$  to  $Q7$  is supplied, the fourth to seventh switching transistors  $Q4$  to  $Q7$  are switched on.



[0183] Fig. 7 is an equivalent circuit schematic of the pixel circuit 50 for the data-writing period T1. For the data-writing period T1, the data current  $I_{data}$  from the data line driving circuit 14 is supplied to the pixel circuit 50 through the data line  $X_m$ . Then, a quantity of electric charge corresponding to the data current  $I_{data}$  is stored in the storage capacitor  $C_n$ . At that time, the first to fifth transistors Qd1 to Qd5 constituting the current control circuit unit 60 in the pixel circuit 50 are mutually connected in parallel as shown in Fig. 7. The resultant gain factor  $\beta_{po}$  of the current control circuit unit 60 in which the first to fifth transistors Qd1 to Qd5 are mutually connected in parallel is  $5\beta_d$ . The electric charges for maintaining this state are stored in the storage capacitor  $C_n$ .

[0184] Next, for the predetermined light-emitting period T2, the first scanning signal SC1 for switching off the first and second switching transistors Q1, Q2 is supplied through the first sub-scanning line  $Y_{n1}$  from the scanning line driving circuit 13. Further, at that time, the second scanning signal SC2 for switching on the third switching transistor Q3 is supplied through the second sub-scanning line  $Y_{n2}$  from the scanning line driving circuit 13. Furthermore, the third scanning signal SC3 for switching off the fourth to seventh switching transistors Q4 to Q7 is supplied through the third sub-scanning line  $Y_{n3}$  from the scanning line driving circuit 13.

[0185] When the first scanning signal SC1 for switching off the first and second switching transistors Q1, Q2 is supplied, the first and second switching transistors Q1, Q2 are switched off, respectively. Further, when the second scanning signal SC2 for switching on the third switching transistor Q3 is supplied, the third switching transistor Q3 are switched on. Furthermore, when the third scanning signal SC3 for switching off the fourth to seventh switching transistors Q4 to Q7 is supplied, the fourth to seventh switching transistors Q4 to Q7 are switched off.

[0186] Fig. 8 is an equivalent circuit schematic of the pixel circuit 50 for the light-emitting period T2. In the current control circuit unit 60 for the light-emitting period T2, the first to fifth transistors Qd1 to Qd5 constituting the current control circuit unit 60 are mutually connected in series. The resultant gain factor  $\beta_{so}$  of the current control circuit unit 60 in which the first to fifth transistors Qd1 to Qd5 are mutually connected in series is  $\beta_d/5$ .

[0187] Also, the pixel circuit 50 generates the driving current  $I_{el}$  from the first to fifth transistors Qd1 to Qd5 mutually connected in series, on the basis of the voltage corresponding to a quantity of electric charge corresponding to the data current  $I_{data}$  stored in the storage capacitor  $C_n$ . Then, by supplying the driving current  $I_{el}$  to the organic EL element

21, the very organic EL element 21 emits light in accordance with the current level of the driving current  $I_{el}$ .

[0188] As a result, advantages similar to those of the first exemplary embodiment can also be obtained from the pixel circuit 50 having the current control circuit unit 60.

[0189] Third Exemplary Embodiment

[0190] Next, applications of the organic EL display device 10 as the electro-optical device described in the first and second exemplary embodiments to electronic apparatuses will be described with reference to Figs. 9 and 10. The organic EL display device 10 can be applied to various electronic apparatuses such as mobile personal computers, mobile phones, or digital cameras.

[0191] Fig. 9 is a perspective view illustrating a configuration of a mobile personal computer. In Fig. 9, the personal computer 70 includes a main body 72 having a keyboard 71, and a display unit 73 employing the organic EL display device 10.

[0192] In this case, the display unit 73 employing the organic EL display device 10 has advantages similar to those of the aforementioned exemplary embodiments.

[0193] Fig. 10 is a perspective view illustrating a configuration of a mobile phone. In Fig. 10, the mobile phone 80 includes a plurality of manipulation buttons 81, an earpiece 82, a mouthpiece 83, and a display unit 84 employing the organic EL display device 10. Further, in this case, the display unit 84 employing the organic EL display device 10 has advantages similar to those of the aforementioned exemplary embodiments.

[0194] Further, the present invention is not limited to the exemplary embodiments described above, but may be implemented as follows.

[0195] In the aforementioned exemplary embodiments, the five driving transistors  $Q_s$ , constituting the driving current generation circuit unit 30, are mutually connected in series, and the five current supply transistors  $Q_p$ , constituting the current supply circuit unit 40, are mutually connected in parallel. As a result, since the data current  $I_{data}$  having the current level higher than that of the driving current  $I_{el}$  is supplied to the pixel circuit 20, the writing time to the storage capacitor  $C_n$  is shortened. Instead, the five driving transistors  $Q_s$ , constituting the driving current generation circuit unit 30, may be mutually connected in parallel, and the five current supply transistors  $Q_p$ , constituting the current supply circuit unit 40, may be mutually connected in series. By doing so, it is possible to implement an electronic device having an amplification function of generating the driving current  $I_{el}$  having a higher current level on the basis of the data current  $I_{data}$  having a small current

level. According to this construction, for example, the data current  $I_{data}$  having a higher current level can be supplied to the pixel circuit 20. As a result, the aforementioned electronic device can be applied to a memory such as MRAM (magneto-resistive element), a detecting device such as a photo-detector, or the like, in addition to the organic EL display device 10.

**[0196]** In the above exemplary embodiments, the driving current generation circuit unit 30 includes the five driving transistors  $Q_s$ . Further, the current supply circuit unit 40 includes the five current supply transistors  $Q_p$ . Instead, the driving current generation circuit unit 30 may include five or more, or five or less driving transistors  $Q_s$ . Further, the current supply circuit unit 40 may include five or more, or five or less current supply transistors  $Q_p$ . By doing so, without reducing the aperture ratio in comparison with the conventional pixel circuit, the data current  $I_{data}$  having the quantity of current larger than the quantity of current of the driving current  $I_{el}$  can be supplied to the pixel circuit 20.

**[0197]** Even when the polarity of the respective transistors is changed in the first and second exemplary embodiments, the similar advantages can be obtained.

**[0198]** Although the organic EL elements 21 are used as the electronic elements in the above exemplary embodiments, any electronic elements, other than the organic EL elements, may be used. For example, electro-optical elements or light emitting elements such as LEDs or FEDs may be used.

**[0199]** Although the organic EL display device 10 using the pixel circuit 20 having the organic EL elements 21 is used as the electronic device in the above exemplary embodiments, a display device using a pixel circuit having inorganic EL elements light emitting layers of which are made of inorganic materials may be used.

**[0200]** Although the organic EL display device 10 in which the pixel circuits 20, 50 having the organic EL elements 21 of only one color are provided is described in the above exemplary embodiments, the present invention may be applied to the organic EL display device in which the pixel circuits 20, 50 for the respective colors are provided in the three-color organic EL elements 21 of red, green and blue.